UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,324	10/10/2001	Giuseppe Rossi	08305-115001 / 20-29	6931

7590 02/09/2005

THOMAS J D'AMICO
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER	
YAM, STEPHEN K	

ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,324	ROSSI, GIUSEPPE	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to Amendments and remarks filed on November 19, 2004. Claims 1-26 are currently pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 3, 4, and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Itani US Patent No. 6,707,492.

Regarding Claim 1, Itani teaches (see Fig. 1 and 7) a method of controlling a gain in a pixel array comprising changing (using (79-81,88-90)) the gain of an amplifier (72, 73) in a gain stage (5) of a sensor (see Fig. 1) in response to a signal (out of (3)) read out from a pixel array (3) in the sensor, wherein said gain stage is in an output path (see Fig. 1) to an analog to digital converter (6) for readout (see Col. 4, line 65 to Col. 5, line 8), and changing the power consumption of the amplifier in the gain stage in response to changing the gain (since the capacitors in the feedback path (see Fig. 7) are utilized according to the switches (79-81) to adjust gain, thereby inherently controlling power consumption, as also demonstrated in Applicant's embodiment in Fig. 2).

Regarding Claim 3, Itani teaches decreasing the power consumption in response to a decrease in the gain and increasing the power consumption in response to an increase in the gain (since inherently, a higher gain requires more power for amplification, and a lower gain requires less power for amplification, when adjusting the amplifier gain and keeping other factors constant).

Regarding Claim 4, Itani teaches associating a plurality of power consumption settings with a plurality of gain settings (since power consumption is dependent on gain), selecting a gain setting from a plurality of gain settings (using (11)), and selecting a power consumption setting (power consumption of amplifier) associated with the selected gain setting.

Regarding Claim 7, Itani teaches each of the plurality of gain settings associated with a different one of the plurality of power consumption settings (since power consumption is dependent on gain).

3. Claims 22-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakano US Patent No. 5,905,256.

Regarding Claim 22, Nakano teaches a method of controlling gain in a pixel array (see Col. 1, lines 11-15) comprising changing the gain of an amplifier (see Fig. 1) in a gain stage of a sensor (see Col. 1, lines 11-15) read out from a pixel array in the sensor, and changing a gain bandwidth (GBW) (see Col. 2, lines 19-20, Col. 3, lines 45-48 and Col. 4, lines 57-59) of the amplifier in the gain state in response to changing the gain (see Col. 4, lines 57-59 and Col. 7, lines 50-56).

Regarding Claim 23, Nakano teaches changing the GBW comprises changing a transconductance (see Col. 4, lines 19-26 and 53-55) of an input transistor (23) in the amplifier.

Regarding Claim 24, Nakano teaches decreasing the GBW in response to a decrease in the gain (since GBW = gain * bandwidth), and increasing the GBW in response to a increase in the gain.

Regarding Claims 25 and 26, RMS noise is always present within an analog electrical system and occupies all frequencies, so therefore decreasing the operating bandwidth decreases the amount of total RMS noise (from cutting off the noise in the deleted frequency bandwidth range) (see also Col. 2, lines 5-8) and decreasing the gain also decreases the amplification amount of the RMS noise, hence decreasing the overall RMS noise level, and for the same reasons, increasing the GBW increases the RMS noise.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itani.

Regarding Claim 5, Itani teaches the method in Claim 4, according to the appropriate paragraph above. Itani does not teach the gain setting selected from eight gain settings. It is well known in the art to select an appropriate number of settings for a system, to provide sufficient adjustability without requiring excessively complex components, and to coordinate the settings

of a system to functionally operate at an optimum level. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide eight gain settings in the method of Itani, to provide an increased level of adjustability for improved precision.

6. Claims 2, 8, 11, and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itani in view of Venes US Patent No. 5,668,501.

Regarding Claims 2, 8, 11, and 13-20, Itani teaches the method in Claim 1, according to the appropriate paragraph above. Regarding Claim 8, Itani also teaches (see Fig. 1 and 7) selecting one of a plurality of gain settings (see Col. 4, lines 49-51 and Col. 4, line 65 to Col. 5, line 17) in response to a signal read out from a pixel array (3) in a sensor (see Fig. 1), with a gain stage (5) as an output path to an analog to digital converter (6) for readout. Itani also teaches the gain stage with a differential amplifier (see Fig. 7). Regarding Claim 18, Itani teaches a pixel array with pixels arranged in rows and columns (CCD- see Col. 3, lines 64-66) and a read-out section (4) operative to read out signals generated by pixels in the pixel array. Itani does not teach changing the power consumption by changing a transconductance of an input transistor in the amplifier by generating two or more bias currents having bias current values associated with the selected gain setting and applying the two or more bias currents to a plurality of parallel transistors in the amplifier to change the input transconductance, or a transconductance controller operative to select an input transconductance of the input transistor in response to a selected gain setting, with first and second parallel transistors connected to a first and second bias supplies, respectively, with a bias current generator to select values for a first and second bias current associated with a selected gain setting, a bias current generator to generate a first and second

current and apply the first and second current to the first and second bias current supplies, wherein each first and second bias current value produces a different input transconductance, with the bias current selector having a plurality of switches to select the gain setting using a set of current values. Venes teaches (see Fig. 4 and 5) a method of controlling gain comprising changing (see Col. 1, lines 62-64 and Col. 2, lines 1-11) the gain of an amplifier in a gain stage in response to a signal (in (1)) (see Fig. 5), and changing the power consumption of the amplifier in the gain stage in response to changing the gain (see Col. 6, lines 30-36), with changing the power consumption by changing a transconductance (see Col. 4, lines 35-51) of an input transistor (T6, T10) in the amplifier (see Col. 6, lines 18-21), by generating two or more bias currents (see Col. 2, lines 45-53) having bias current values associated with the selected gain setting (see Col. 2, lines 52-53), and applying said two or more bias currents to a plurality of parallel transistors (T6, $T6_1$,..., $T6_N$, T10, $T10_1$, ..., $T10_N$) (see Fig. 1) in an amplifier in a gain stage in order to change the input transconductance of the amplifier (see Col. 4, lines 40-51 and Col. 6, lines 51-58), with a gain selector ($S3_1$... $S3_m$) and a transconductance controller (40, $S1_1$... $S1_N$, $S2_1$... $S2_N$) operative to select an input transconductance of the input transistor in response to a selected gain setting (see Col. 6, lines 47-58), the input transistor comprising a first plurality of parallel transistors (T6, $T6_1$,..., $T6_N$) (see Fig. 1) connected to a first bias current supply (T1, T5) ("first current mirror"- see Col. 3, lines 54-62), and a second plurality of parallel transistors (T10, $T10_1$, ..., $T10_N$) (see Fig. 1) connected to a second bias current supply ("third current mirror"- see Col. 4, lines 5-16), with the transconductance controller comprising a bias current selector (see Col. 6, lines 47-51) operative to select values for a first bias current and a second bias current associated with a selected gain setting, and a bias current generator

(generating binary transconductance control signal- see Col. 6, lines 47-51) operative to generate a first current (control signals for (S1, $S1_1$,..., $S1_N$)) having the selected value for the first bias current value and apply said first current to the first bias current supply and to generate a second current (control signals for (S2, $S2_1$,..., $S2_N$)) having the selected value for the second bias current value and apply the second current to the second bias current supply (see Col. 4, lines 42-45), each first and second bias current values producing a different input transconductance (see Col. 4, lines 45-51), with the bias current selector including a plurality of switches ($S1_1$... $S1_N$, $S2_1$... $S2_N$) and operative to select a different set of switches for each of said plurality of gain settings (see Col. 4, lines 40-51), with the bias current selector operative to select a set of current values in response to the switches selected by the gain selector (see Col. 6, lines 51-58), with the transconductance controller comprising a gain decoder (determining (7)) (see Col. 6, lines 47-51) operative to select one or more bias current values in response to a selected gain response from a plurality of bias current values, and a bias generator (outputting (7)) operative to generate and apply said one or more bias current values to at least one of the first and second bias current supplies (see Fig. 1 and 4), and the transconductance controller operative to increase the transconductance of the input transistor in response to an increase in the gain of the differential amplifier and to decrease the transconductance of the input transistor in response to a decrease in the gain of the differential amplifier (see Col. 6, lines 51-58). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the gain adjustment configuration by modifying the input transconductance of input transistors, as taught by Venes, in the method and apparatus of Itani et al., to increase the stability of the amplifier depending on gain and bandwidth conditions, as taught by Venes (see Col. 2, line 63 to Col. 3, line 4).

7. Claims 6, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itani (in view of Venes for Claims 9, 10, and 12) in view of Nakano.

Regarding Claims 6, 9, 10, and 12, Itani (in view of Nakano for Claims 9, 10, and 12) teach the method in Claims 5, 8, and 11, according to the appropriate paragraph above. Itani does not teach selecting from three power consumption settings, each of the three power consumption settings being associated with a different plurality of gain settings, or associating each of a plurality of input transconductance settings to a plurality of gain settings, each input transconductance setting being associated with a given set of bias current values. Nakano teaches a similar method, with selecting from several power consumption settings (see Fig. 1 and 7-9) or input transconductance settings (see Col. 4, lines 19-26 and 53-55), each associated with a different plurality of gain settings (see Col. 9, lines 6-19), each input transconductance setting being associated with a given set of bias current values (see Col. 4, lines 50-55 and Col. 8, lines 5-7, 28-30). In addition, it is well known in the art to select an appropriate number of settings for a system, to provide sufficient adjustability without requiring excessively complex components, and to coordinate the settings of a system to functionally operate at an optimum level. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide three power consumption settings, with each power consumption setting associated with a different plurality of gain settings and each of the plurality of gain settings associated with a different one of the plurality of power consumption and input transconductance settings, as taught by Nakano, in the method of Itani (in view of Venes where appropriate), to provide an

increased and appropriate level of adjustability for improved power usage, as taught by Nakano (see Col. 4, lines 42-49).

8. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Itani in view of Venes, further in view of Mathur et al. US Patent No. 6,661,457.

Regarding Claim 21, Itani in view of Venes teaches the sensor in Claim 18, according to the appropriate paragraph above. Itani does not teach the sensor as an active pixel sensor (APS). Mathur et al. teach (see Fig. 1, 3, 6) a sensor having an active (APS) pixel array (10) (see Col. 5, lines 38-42) having pixels arranged in rows and columns (see Fig. 2) and a gain stage (82) having an amplifier with a changing gain (see Col. 7, lines 50-53) for a signal read out from the pixel array using a readout circuit (12). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use an active pixel array for the sensor as taught by Mathur et al. in the sensor of Itani in view of Venes, to provide independent/individual pixel circuitry for reducing noise and interference from adjacent pixels.

Response to Arguments

9. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Azim US Patent No. 6,137,533 teaches a method of controlling a gain in a pixel array with changing the gain of an amplifier in response to a signal read out from a pixel array (102) in the sensor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (571)272-2449. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Porta can be reached on (571)272-2444. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SY

SY

THANH X. LUU
PATENT EXAMINER